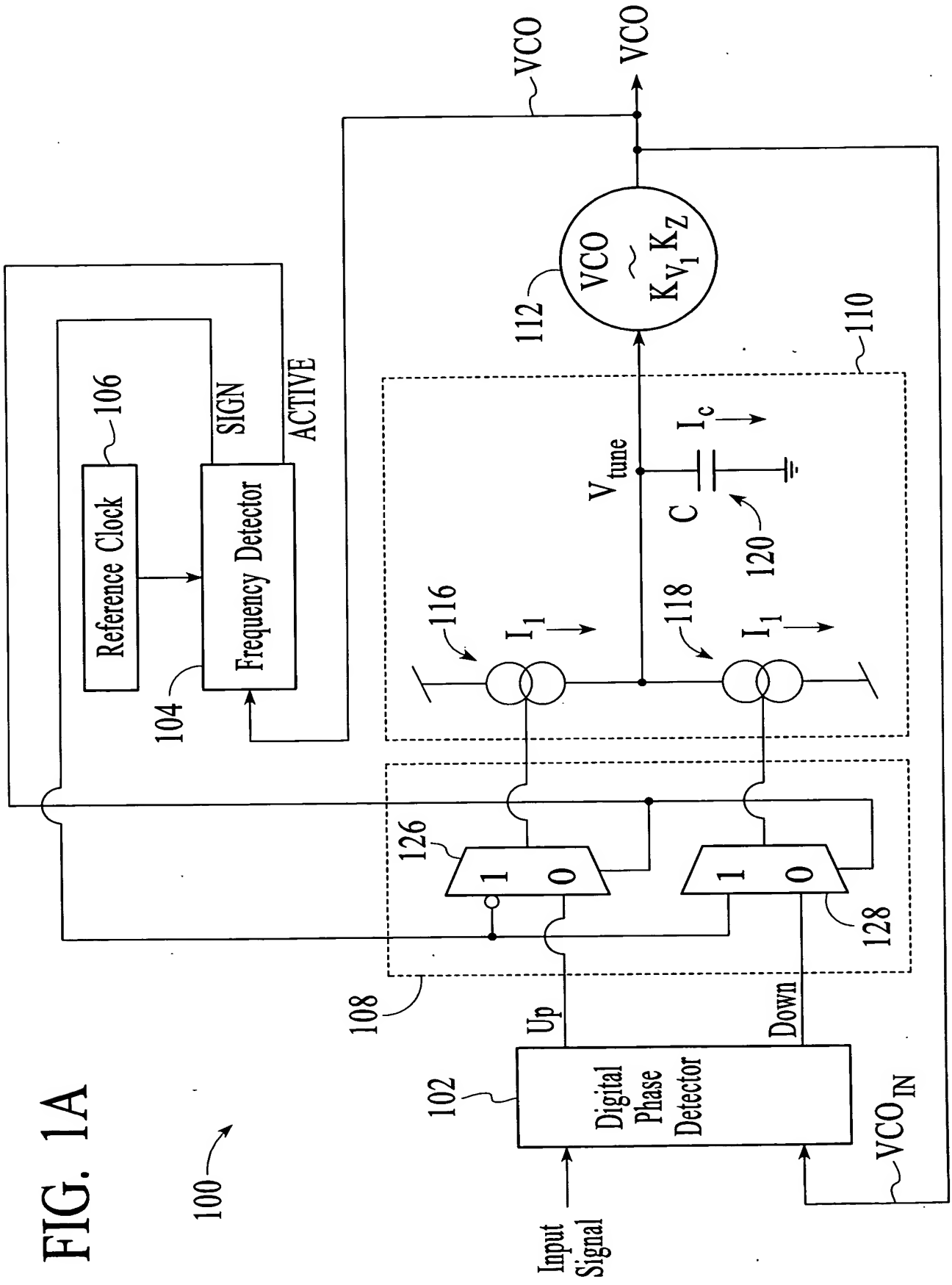

VCO
VCO
112
VCO
$K_{V_1}K_Z$
110
V_{tune}
I_c
C
120
116
I_1
118
I_1
126
1
0
1
0
128
108
Up
Down
102
Digital
Phase
Detector
VCO_{IN}
Input
Signal
100
Reference Clock
106
SIGN
ACTIVE
Frequency Detector
104

FIG. 1A

UP	DOWN	SIGN	ACTIVE	I_c
X	X	1	1	$-I_1$
X	X	0	1	$+I_1$
1	0	X	0	$+I_1$
0	1	X	0	$-I_1$

FIG. 1B

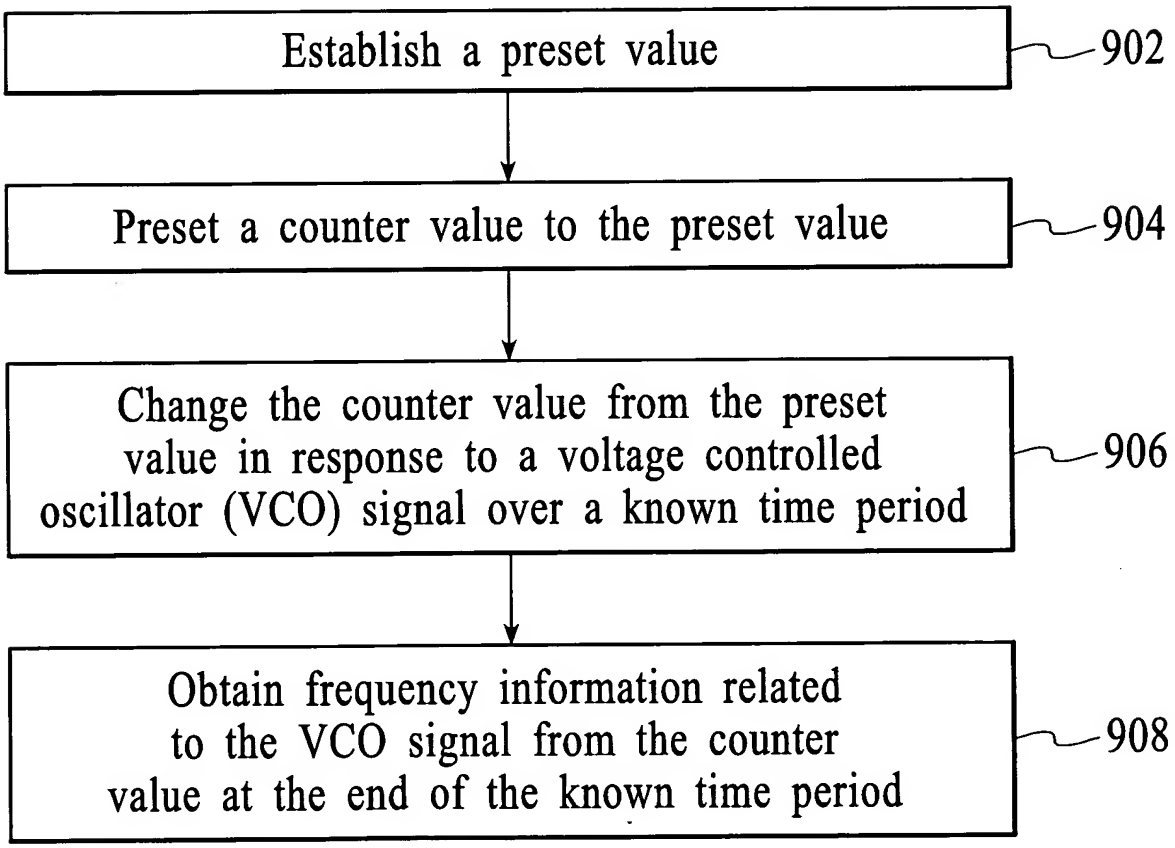


FIG. 9

FIG. 2

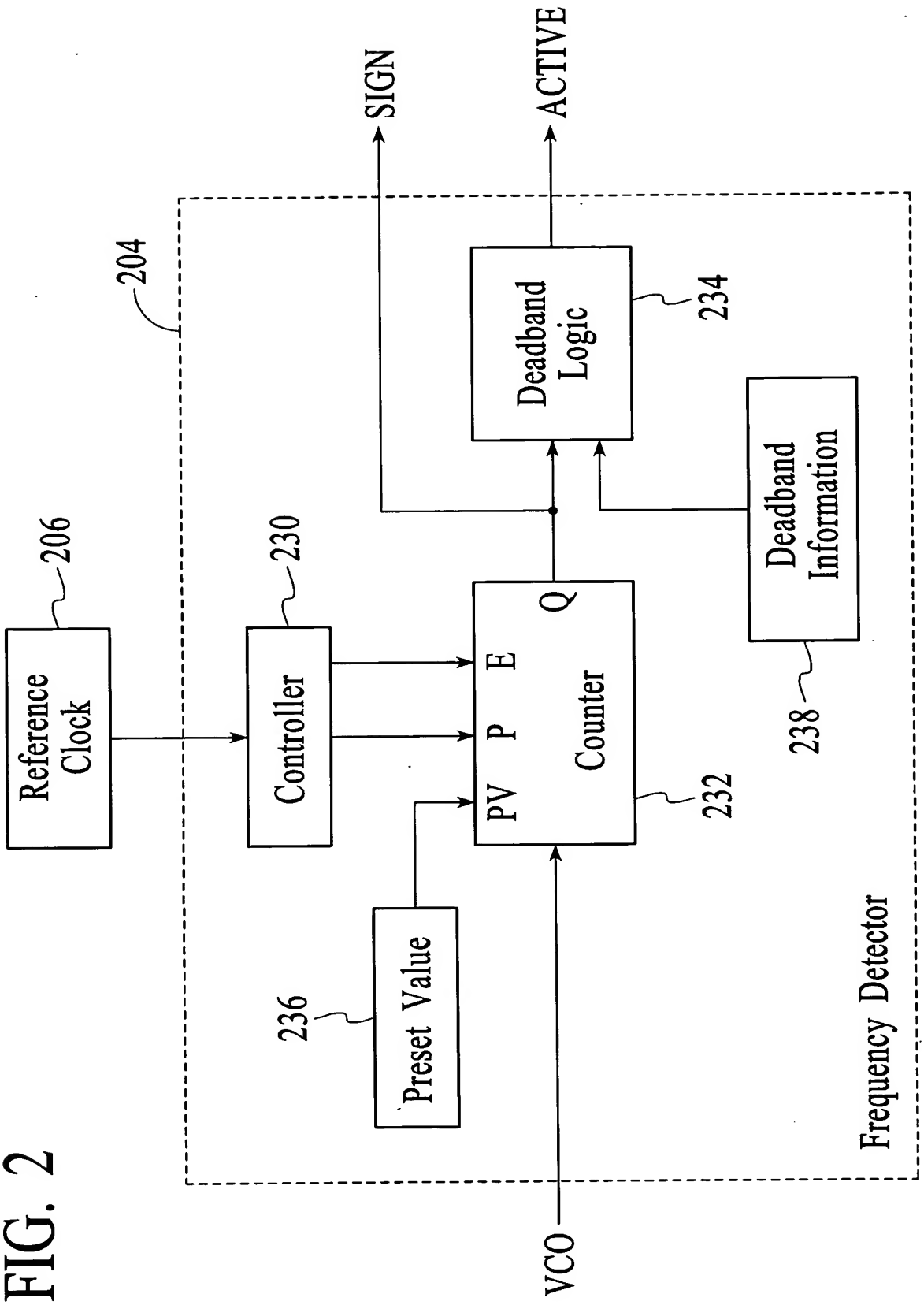
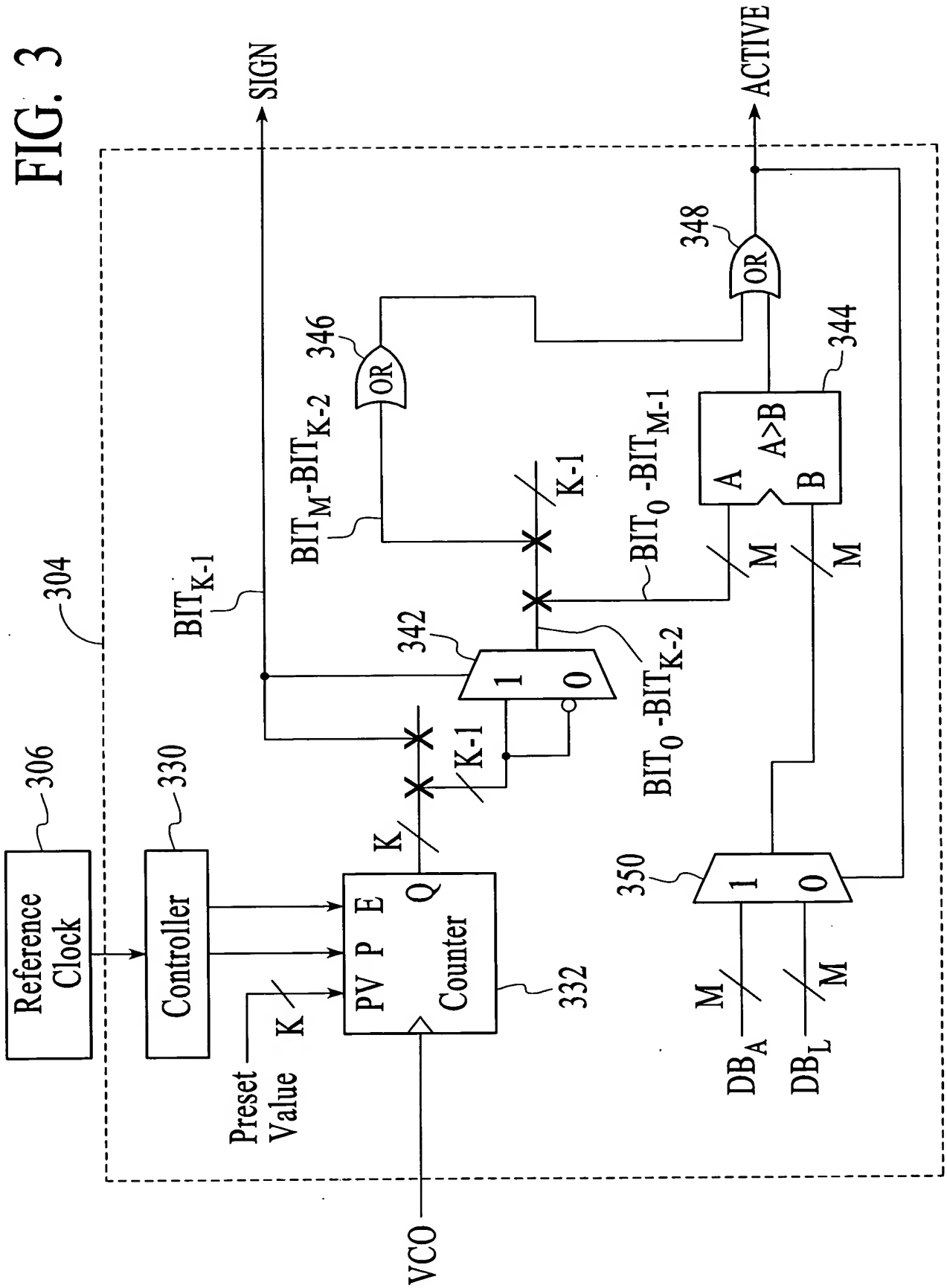

SIGN
ACTIVE
204
Deadband Logic
234
Deadband Information
238
Reference Clock
206
Controller
230
PV P E Q
Counter
232
Preset Value
236
VCO
Frequency Detector

FIG. 3


SIGN
ACTIVE
304
306
330
Reference Clock
Controller
Preset Value
K
PV P E
Q
Counter
332
VCO
K
K-1
342
1
0
BIT_{K-1}
BIT_M-BIT_{K-2}
346
OR
BIT_0 -BIT_{K-2}
BIT_0 -BIT_{M-1}
348
OR
344
A
A>B
B
M
M
350
1
0
M
M
DB_A
DB_L

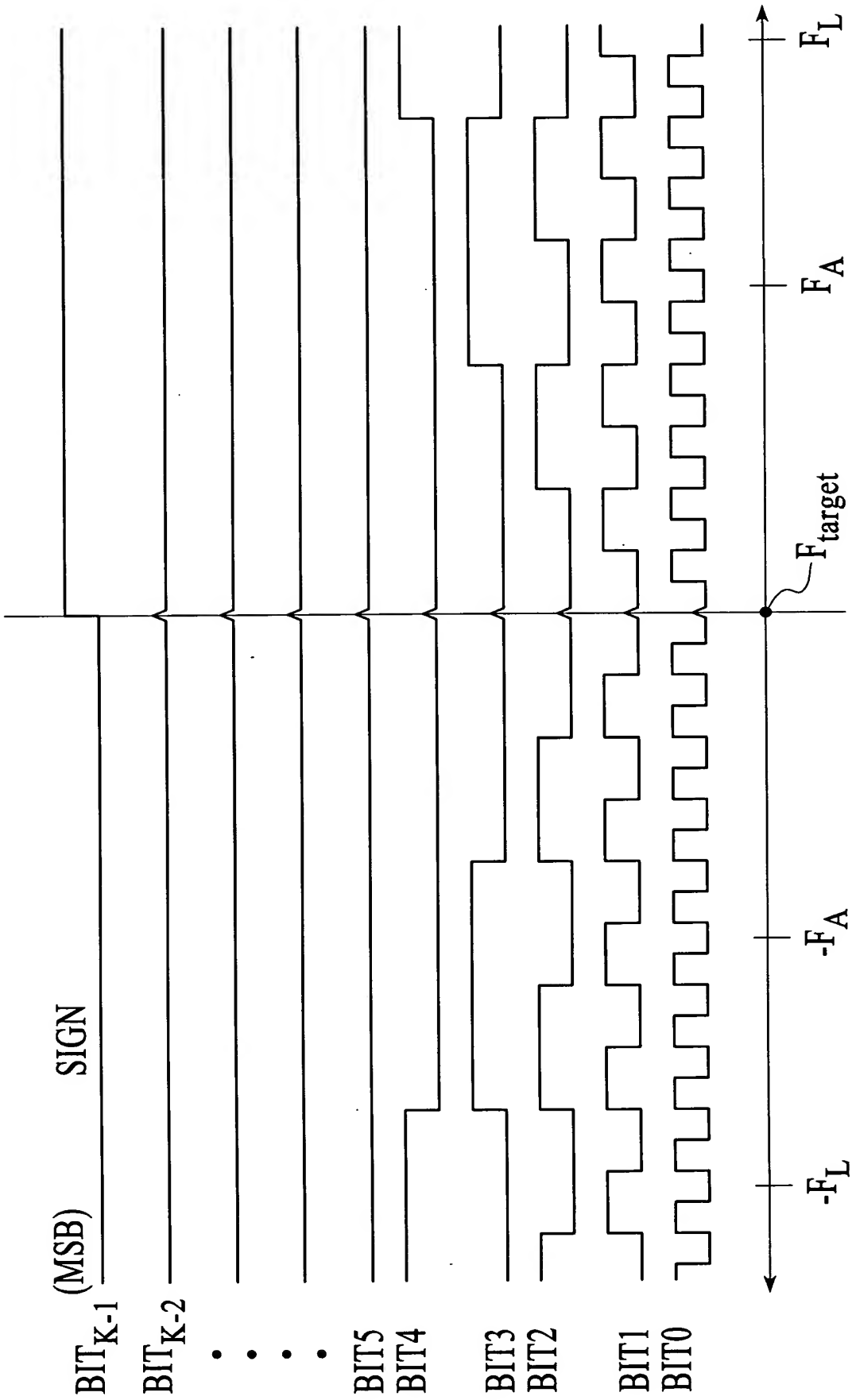

(MSB)
SIGN
BIT_{K-1}
BIT_{K-2}
BIT5
BIT4
BIT3
BIT2
BIT1
BIT0
F_L
F_A
F_{target}
$-F_A$
$-F_L$

FIG. 4

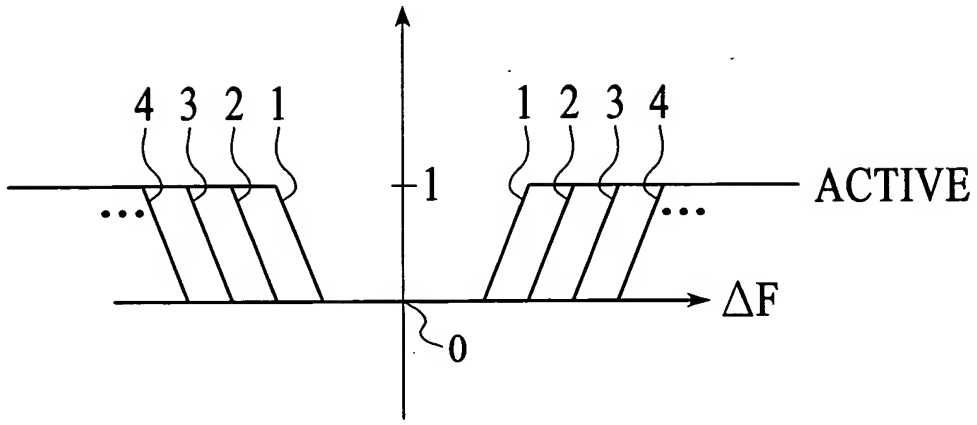


FIG. 5A

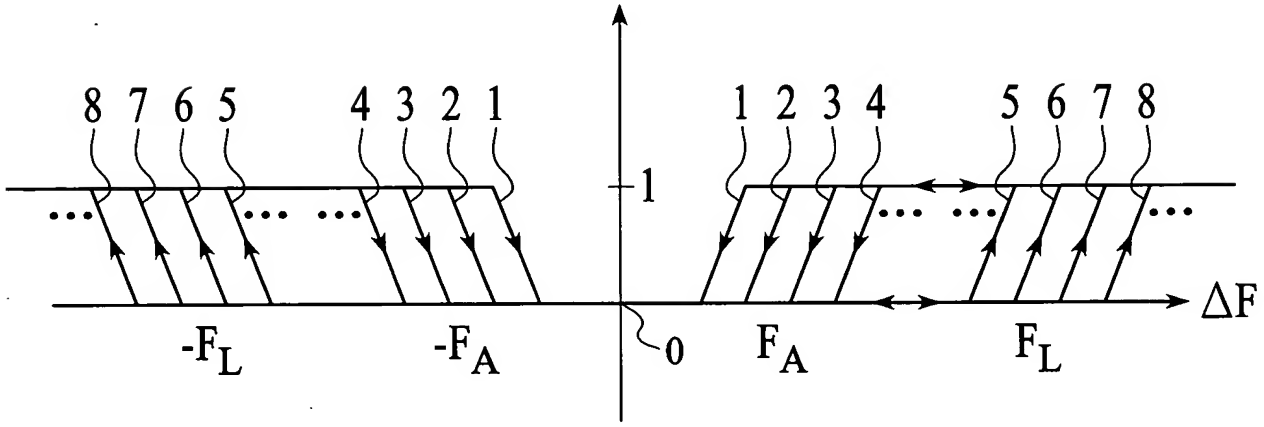


FIG. 5B

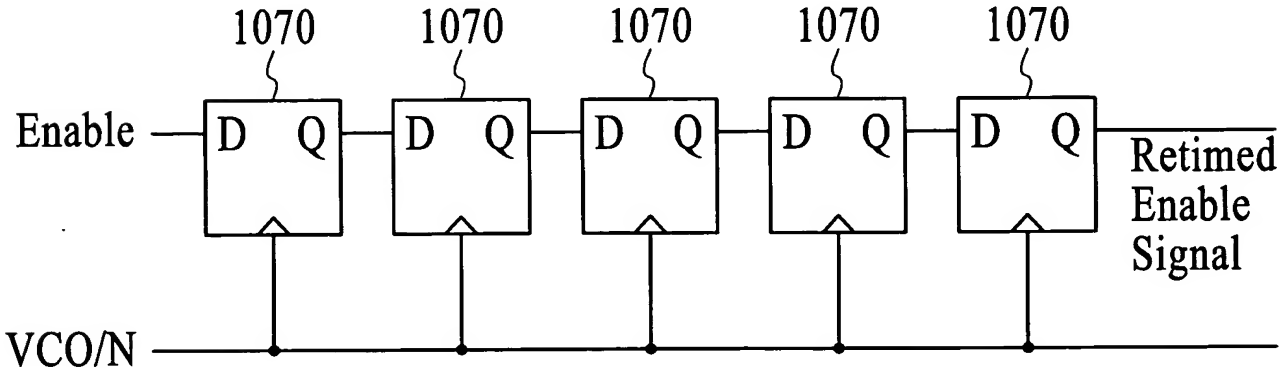


FIG. 10

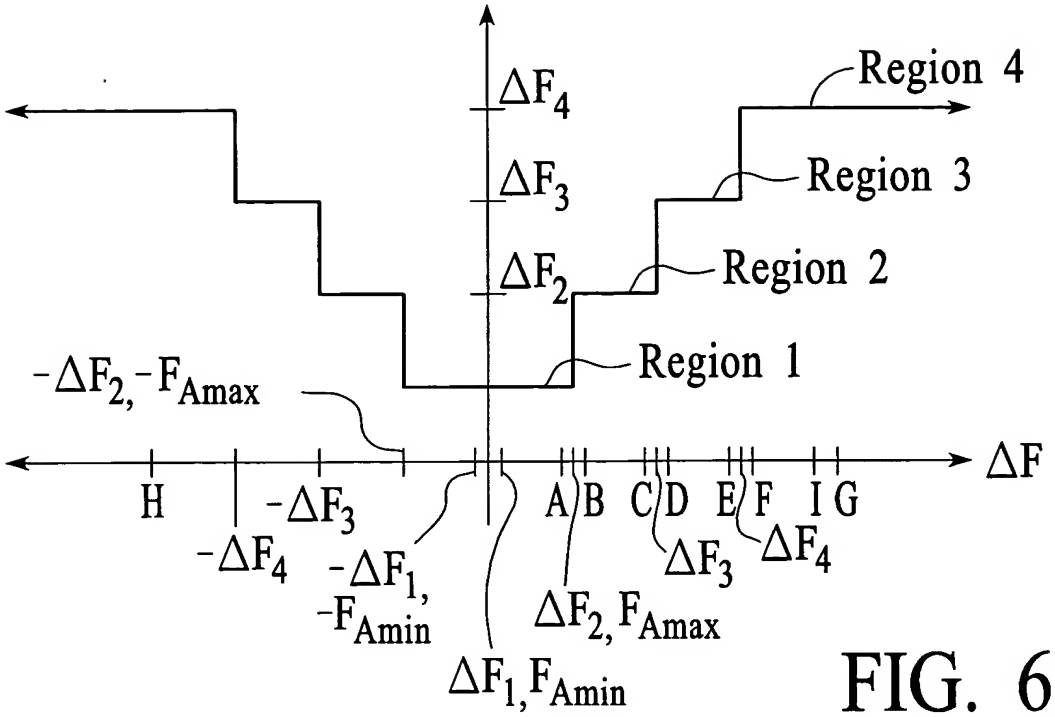

ΔF4
ΔF3
ΔF2
Region 4
Region 3
Region 2
Region 1
-ΔF2,-FAmax
ΔF
H
-ΔF3
-ΔF4
-ΔF1,
-FAmin
ΔF1,FAmin
A
B
C
D
E
F
I
G
ΔF2,FAmax
ΔF3
ΔF4

FIG. 6

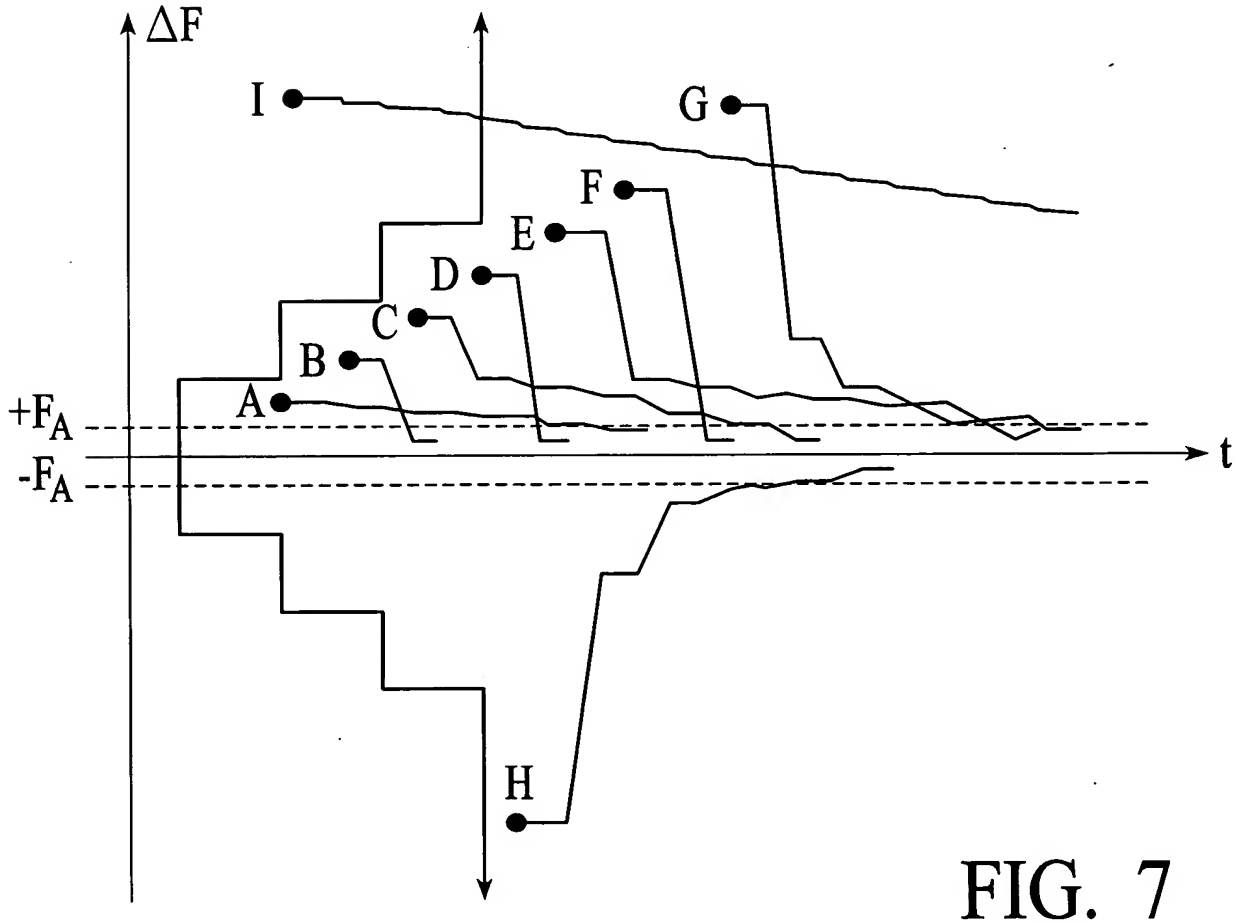

ΔF
I
G
F
E
D
C
B
A
+FA
-FA
t
H

FIG. 7

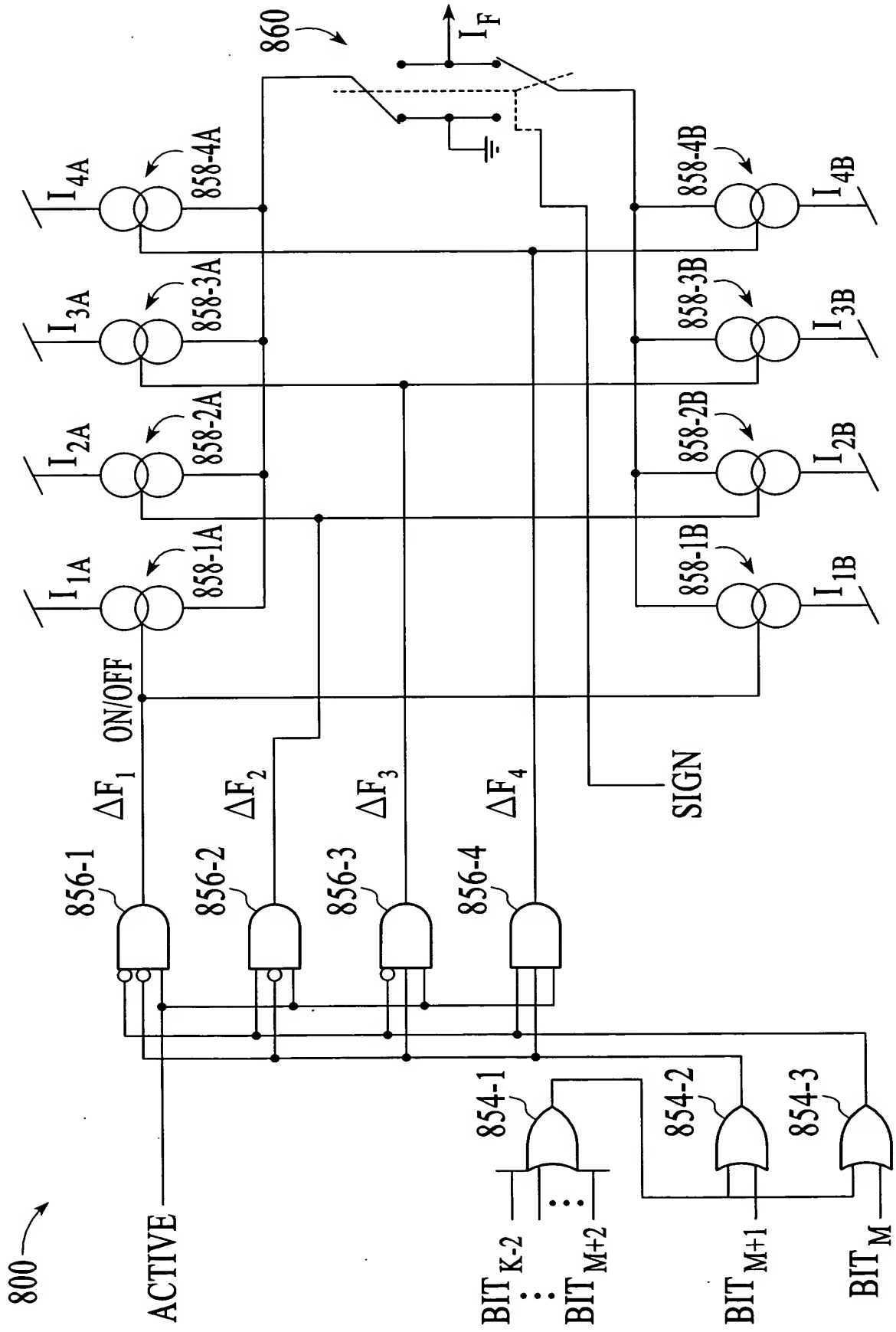

800
ACTIVE
ON/OFF
ΔF_1
ΔF_2
ΔF_3
ΔF_4
856-1
856-2
856-3
856-4
854-1
854-2
854-3
BIT_{K-2}
BIT_{M+2}
BIT_{M+1}
BIT_M
From FIG. 3
SIGN
860
I_F
I_{1A}
I_{2A}
I_{3A}
I_{4A}
858-1A
858-2A
858-3A
858-4A
I_{1B}
I_{2B}
I_{3B}
I_{4B}
858-1B
858-2B
858-3B
858-4B

FIG. 8